CLAIMS

What is claimed is:

1. A flash memory controller comprising:

a processor for receiving at least one request from a host system; and

an index comprising information regarding sectors of a flash memory, wherein the processor can utilize the index to determine the sectors of the flash memory that are available for programming, reprogramming, or reading, wherein the host system interacts with the flash memory controller without the host system having information regarding the configuration of the flash memory.

2. The flash memory controller of claim 1 wherein the at least one request comprises a logical block address for reading or writing and wherein the index maps the logical block address to a physical block address in the flash memory.

3. The flash memory controller of claim 1 further comprising a first-in-first-out unit (FIFO) for recycling obsolete sectors so that they are available for reprogramming.

4. The flash memory controller of claim 3 wherein the FIFO recycles obsolete sectors in the background with respect to the host system to free up resources of the host system.

5. The flash memory controller of claim 1 further comprising a Universal Serial Bus interface to the host system.

6. The flash memory controller of claim 1 wherein the flash memory controller and the flash memory function as a hard disk and/or hard disk equivalent for the host system.

7. The flash memory controller of claim 1 wherein the processor utilizes SCSI protocols to interface with the flash memory.

8. The flash memory controller of claim 1 wherein the index comprises a look-up table.

9. The flash memory controller of claim 1 wherein the index comprises a physical usage table.

10. The flash memory controller of claim 1 wherein the flash memory controller can be applied to USB and ExpressCard plug and receptacle systems.

11. The flash memory controller of claim 1 wherein the flash memory controller can be applied to multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) plug and receptacle systems.

12. The flash memory controller of claim 1 wherein the flash memory controller provides multiple-block data access.

13. The flash memory controller of claim 1 wherein the flash memory controller provides dual channel processing.

14. The flash memory controller of claim 1 wherein the flash memory controller can perform multiple banks interleave.

15. The flash memory controller of claim 1 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

16. A system comprising:

a first processor;

a device interface coupled to the processor; and

a memory controller coupled to the device interface, the memory controller comprising:

a second processor for receiving at least one request from a host system; and

an index comprising information regarding sectors of a flash memory, wherein the second processor can utilize the index to determine the sectors of the flash memory that are available for programming, reprogramming, or reading, wherein the host system interacts with the flash memory controller without the host system having information regarding the configuration of the flash memory.

17. The system of claim 16 wherein the at least one request comprises a logical block address for reading or writing and wherein the index maps the logical block address to a physical block address in the flash memory.

18. The system of claim 16 further comprising a first-in-first-out unit (FIFO) for recycling obsolete sectors so that they are available for reprogramming.

19. The system of claim 18 wherein the FIFO recycles obsolete sectors in the background with respect to the host system to free up resources of the host system.

20. The system of claim 16 further comprising a Universal Serial Bus interface to the host system.

21. The system of claim 16 wherein the flash memory controller and the flash memory function as a hard disk and/or hard disk equivalent for the host system.

22. The system of claim 16 wherein the processor utilizes SCSI protocols to interface with the flash memory.

23. The system of claim 16 wherein the index comprises a look-up table.

24. The system of claim 16 wherein the index comprises a physical usage table.

25. The system of claim 16 wherein the flash memory controller can be applied to USB and ExpressCard plug and receptacle systems.

26. The system of claim 16 wherein the flash memory controller can be applied to multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) plug and receptacle systems.

27. The system of claim 16 wherein the flash memory controller provides multiple-block data access.

28. The system of claim 16 wherein the flash memory controller provides dual channel processing.

29. The system of claim 16 wherein the flash memory controller can interleave multiple blocks.

30. The system of claim 16 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

31. A method for managing flash memory, the method comprising:

(a) receiving at least one request from a host system utilizing a processor within a memory controller; and

(b) determining which sectors of the flash memory are available for programming, reprogramming, or reading utilizing the processor and an index within the memory controller, wherein the host system interacts with the flash memory controller without the host system having information regarding the configuration of the flash memory.

32. The method of claim 31 wherein the determining step (b) comprises (b1) mapping a logical block address, which is provided in the at least one request from the host system, to a physical block address in the flash memory utilizing the index.

33. The method of claim 31 further comprising (c) recycling obsolete sectors so that they are available for reprogramming.

34. The method of claim 33 wherein the recycling step (c) occurs in the background with respect to the host system to free up resources of the host system.

35. The method of claim 33 wherein the recycling step (c) comprises:

(c1) block copying valid data from sectors of a first block to sectors of a second block, wherein the sectors of the first block become obsolete sectors; and

(c2) erasing the obsolete sectors of the first block so that they are available for reprogramming.

36. The method of claim 31 wherein the method can be applied to USB and ExpressCard plug and receptacle systems.

37. The method of claim 31 wherein the method can be applied to multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) plug and receptacle systems.

38. The method of claim 31 wherein the flash memory controller provides multiple-block data access.

39. The method of claim 31 wherein the flash memory controller provides dual channel processing.

40. The method of claim 31 wherein the flash memory controller can interleave multiple blocks.

41. The method of claim 31 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.

42. A computer readable medium containing program instructions for managing flash memory, the program instructions which when executed by a computer system cause the computer system to execute a method comprising:

(a) receiving at least one request from a host system utilizing a processor within a memory controller; and

(b) determining which sectors of the flash memory are available for programming, reprogramming, or reading utilizing the processor and an index within the memory controller, wherein the host system interacts with the flash memory controller without the host system having information regarding the configuration of the flash memory.

43. The computer readable medium of claim 42 wherein the determining step (b) comprises program instructions for (b1) mapping a logical block address, which is provided

in the at least one request from the host system, to a physical block address in the flash memory utilizing the index.

44. The computer readable medium of claim 42 further comprising (c) program instructions for recycling obsolete sectors so that they are available for reprogramming.

45. The computer readable medium of claim 44 wherein the recycling step (c) occurs in the background with respect to the host system to free up resources of the host system.

46. The computer readable medium of claim 44 wherein the recycling step (c) comprises program instructions for:

(c1) block copying valid data from sectors of a first block to sectors of a second block, wherein the sectors of the first block become obsolete sectors; and

(c2) erasing the obsolete sectors of the first block so that they are available for reprogramming.

47. The computer readable medium of claim 42 wherein the computer readable medium can be applied to USB and ExpressCard plug and receptacle systems.

48. The computer readable medium of claim 42 wherein the computer readable medium can be applied to multi-mode USB, Secure Digital (SD), MultiMediaCard (MMC), Memory Stick (MS), and Compact Flash (CF) plug and receptacle systems.

49. The computer readable medium of claim 42 wherein the flash memory controller provides multiple-block data access.

50. The computer readable medium of claim 42 wherein the flash memory controller provides dual channel processing.

51. The computer readable medium of claim 42 wherein the flash memory controller can interleave multiple blocks.

52. The computer readable medium of claim 42 wherein the flash memory controller can perform functions of multiple block access, multiple bank interleaving, and multiple channel operations in a memory access cycle.